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(54) **Memory test method and nonvolatile memory with low error masking probability**

(57) A nonvolatile memory device (10) has a signature code generator (14, 15, 17) generating a present signature code (Q) from an algorithm modified dynamically as a function of predefined varying parameters. A variable parameter may be the address (A) of a memory cell being addressed; in this case the output of the code generator (Q) is a function of data (D) read from the cell array (24), the previously calculated signature code (Q)

and the address of the read data. The data are read in sequence, using an internal clock (CK) generated by an internal clock oscillator (11). In test mode, the memory is scanned sequentially, beginning from any memory location, selected randomly, and the signature code (Q) varies in dynamic way; at the end of memory scanning, the signature code (Q) is compared to an expected result.

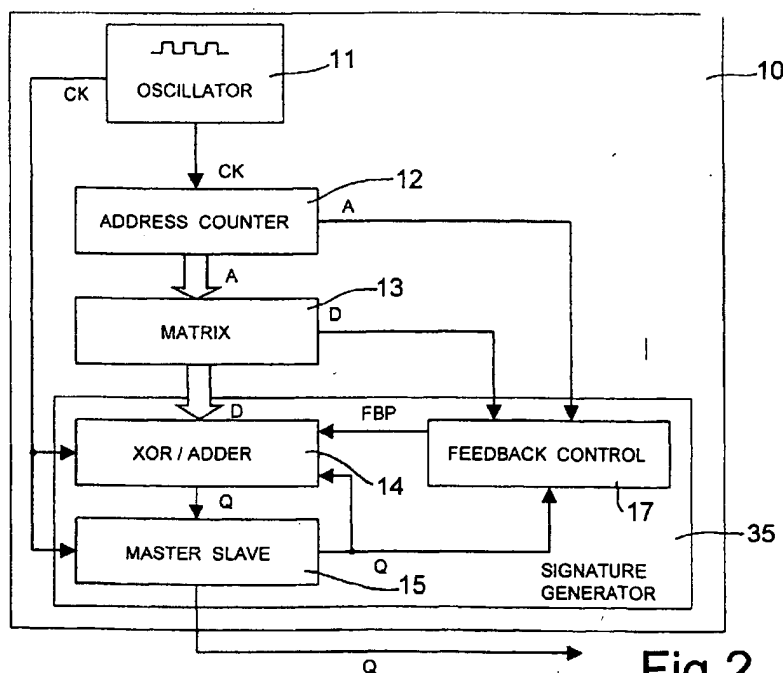


Fig.2

Description

[0001] The present invention relates to a memory test method and to a nonvolatile memory with low error masking probability. In particular, the invention relates to flash memories.

[0002] As known, memory test methods are intended to cover and screen various types of possible defects present in memories, so as to ensure reliability of the end product. Memory tests are carried out at different manufacturing stages of the memory using special equipments, exploiting special internally implemented test modes. Memory tests are typically performed, e.g., at Wafer Sort Level, Final Test Level and Final Device Characterization Level.

[0003] Specifically, the Wafer Sort Level test is carried out by connecting one or more memories belonging to a same wafer to a test machine which generates the addresses and timing clocks fed to each tested memory in the wafer; then a test pattern is written in each tested memory; data are read from each memory and furnished to the test machine to be compared with expected readings, to detect any fault.

[0004] The wafer sort level testers are limited in the array scanning speed; in particular, most of the memory testers provide the facility of multiple strobes in a same cycle time (synchronous mode testing, e.g., burst mode testing), which allows to perform data check reading of more than one address location in a same cycle time. Indeed, presently burst mode testing works on the principle of outputting the data read from the matrix in a pipeline way. The matrix array is divided into two independent halves called even and odd matrices, each having a respective set of 16 sense amplifiers for reading. During the device testing, reading is commanded by the tester, which furnishes the beginning address for starting the burst, and a clock RD for synchronization. Then, the memory generates consecutive addresses synchronized with read requests fed to the device through the clock RD. The addresses are decoded separately for the two matrix parts and reading is controlled by even/odd priority signals generated by a timing control logic in the memory. The addresses are linearly incremented in synchronization with the external clock RD and sequence reading is continued until the tester initiates a new burst sequence by latching a new address into the memory through a pin ALE provided for the purpose.

[0005] To test the correct device functionality and screen any possible sensing marginalities, a large number of tests are performed at various stages of Wafer Sort Flow, each needing to scan the whole matrix at least once. Therefore the test time during production is huge. Furthermore the minimum obtainable cycle time at Wafer Sort Level is limited, in the best case, to 100 ns, which is much larger than the access time specification of present flash memories. Thus, testing cannot be made at the memory operative speed. On the other hand, some defects may be detected only at high speed

cycling, because otherwise the possible noise conditions do not intervene or get unnoticed.

[0006] To reduce the test time, the read data are often compressed internally to the device and the compression result, defining a code and also called "signature", is fed to the test machine and compared to an expected result. Thus, the tester does not need to receive all read data, but only a final code (the signature) that is uniquely evaluated as a function of the read data and the sequence in which it occurs; thereby the signatures obtained after a partial or a complete matrix scan flag the possible errors occurred during scanning.

[0007] According to a widespread solution, used in particular for ROMs and called checksum method, the memory array is internally read in a random manner using LFSRs (Linear Feedback Shift Registers) for generating random addresses; at each scan, the read data are summed in a binary way to the previous result; so, if a ROM to be checked consists of 2^N data words and each data word contains B bits, the checksum is formed by the modulo- 2^k arithmetic sum of the 2^N data words in the ROM, where k is arbitrary. This means that all words in ROM are added together and k least significant terms of the sum form the signature or checksum. The result (signature) is fed at preset intervals or at the end of matrix scan to the tester to be compared for finding any failures.

[0008] Another popular solution particularly used for SRAM/DRAMs uses the LFSRs to generate random addresses and data pattern. The internal verification consists of two steps for every randomly addressed location. In the first step, the random data is written at the random address generated. The second step confirms the data back by reading. In some other approaches the data read are compressed in a response analyzer. The compression algorithm is fixed for the entire duration of the matrix scan. Thereby, at any time, the signature $Q(t)$ present in the compressor unit may be mathematically expressed by:

$$Q(t) = f(\text{data}, Q(t-1)) \quad (1)$$

wherein *data* is the just read data and $Q(t-1)$ is the previous signature code.

[0009] A block diagram of a known memory device showing the essential elements as regards testing is shown in Figure 1. The memory device 1 comprises an address counter 2 receiving from the tester an initial address A0 and a synchronization signal RD and generating a sequence of reading addresses A; a matrix 3 receiving from the address counter 2 each time an address A of the cell to be read; an XOR/ADDER block 4, receiving from the matrix 3 the read data D and generating the signature Q; a master/slave unit 5, storing the signature Q and having an output 6 for connection to the tester. A feedback control block 7 generates the feedback polynomial value FBP used by the XOR/ADDER

block 4 to generate the signature Q according to the expression (1); to this end, the feedback control block 7 receives the signature Q. The signature Q is also fed to the XOR/ADDER block 4. XOR/ADDER block 4, master/slave unit 5 and feedback control block 7 form a signature generator 8. The clock RD, fed from the tester, is also used for synchronizing the XOR/ADDER block 4 and the master/slave unit 5.

[0010] The above described compression solution does not always ensure error detection; indeed, the possibility of obtaining the same signature from two different patterns is low but cannot be ruled out.

[0011] Later tests, carried out at Final Test Level or Final Device Characterization Level use high speed machines capable of detecting fault conditions not discovered at Wafer Sort Level. However, also the test machines used at final test level prove to be insufficient to truly satisfy the fast speed test requirements, so that complete memory test cannot be performed in production testing. Furthermore, any defective memories detected at those late stages cause higher costs for rejected devices.

[0012] The aim of the present invention is therefore to provide a test method with improved robustness against error masking.

[0013] According to the present invention, there are provided a test method and a nonvolatile memory device, as defined in Claim 1 and, respectively, 8.

[0014] For a better understanding of the present invention, a preferred embodiment is now described, purely by way of nonlimiting example, with reference to the attached drawings, wherein:

- Figure 1 is a block diagram of a known memory device, showing only the parts involved during testing;
- Figure 2 is a block diagram of the memory device according to the present invention, showing only the parts involved during testing;
- Figure 3 is a block diagram of the memory device architecture according to the present invention as connected to a tester;
- Figure 4 is more detailed block diagram of the memory device according to the present invention;
- Figure 5 shows a circuit implementation of a part of the memory device of Figure 2; and
- Figures 6 and 7 shown the implementation of some parts of Figure 5.

[0015] A memory device 10 according to the invention has the architecture shown in Figure 2. As shown, the memory device 10 has a built-in oscillator 11 generating a clock CK fed to an address counter 12 connected to a matrix 13. The read data D is furnished to a XOR/ADDER block 14 also receiving a feedback polynomial value FBP and a signature Q; the signature Q is fed to a master/slave unit 15, analogously to Figure 1. In Figure 2, the address counter 12 is also connected to the feedback control block 17 and feeds thereto the address

D (or a preset combination/part thereof) for dynamically changing the feedback polynomial during matrix scan, as discussed in detail hereinbelow. XOR/ADDER block 14, master/slave unit 15 and feedback control block 17 form a signature generator 35.

[0016] During testing, when so enabled by a tester not shown, the address counter 12 generates a consecutive sequence of cell addresses to allow a consecutive scanning of a substantial part of the matrix, wherein "substantial" here indicates a number of cells greater than 4, for example an entire sector, if the matrix is divided in sectors, or a matrix half, if the matrix is divided in two parts. Preferably, testing comprises uninterrupted scanning of the entire matrix, so as to reduce the overall testing time.

[0017] Thereby, the total matrix scan time is reduced by a factor of 5-10, depending upon the memory speed. The matrix can be tested at high frequency at Wafer Sort Level, starting from any address, in working-like conditions. Thus, testing is more thorough than presently and defective memories may be detected at an earlier stage.

[0018] Furthermore, the compression algorithm is changed dynamically using the address of the presently selected cell or a signal derived therefrom. Therefore, the compression is no more fixed, but is a function of a predefined variable parameter and the signature may be mathematically expressed by:

$$Q(t) = f(\text{address}, \text{data}, Q(t-1)) \quad (2)$$

[0019] Since the address changes for each memory location, the compression algorithm continuously changes its characteristics reducing the risk of possible error masking.

[0020] The architecture of the memory device 10 according to the invention and its connection to a tester are shown in the diagram of Figure 3. The memory device 10 has an interface 20 connected to input pins 21a-21d including a pin 21a for an address latch enable signal ALE, pins 21b for the addresses ADDRS, a pin 21c for an external clock RD and a pin 21d for a chip enable signal CEN, and pins 21e for input/output data I/O. Signals ALE, ADDRS are fed to the address counter 12; signal CEN (for chip deselection) is fed to all input/output buffers (in a not shown manner) and a burst timing control block 22 generating, as described hereinbelow with reference to Figure 4, timing signals for the memory device 10; and the external clock RD is fed to a clock multiplexer 28. The multiplexer 28 is formed by two clock pass gates 28a and 28b receiving a test mode signal TM and an inverted test mode signal TMN generated by a test mode control unit 30 so as to be alternately conductive. The signal input of the clock pass gate 28a receives the external clock RD; the signal input of the clock pass gate 28b receives the internal clock CK generated by the oscillator 11; the signal outputs of the clock pass gates 28a and 28b are connected to a common clock

node 31 connected to the burst timing control block 22; thus the burst timing control block 22 receives a timing clock CK' selectively fed by the external clock pin 21c or the oscillator 11, according to the value of the test mode signals TM, TMN. Preferably, oscillator 11 is a multifrequency one, and is controlled by the test mode control unit 30 through a frequency control signal F_C as discussed hereinbelow.

[0021] Matrix 13 is shown split in three parts: a decoding stage 23, connected to the address counter 12 to receive the addresses of the cell to be read; a cell array 24, formed by nonvolatile cells 26 to be read (only one shown); and a sensing stage 25, connected to the array 24 and outputting the read data. Structure and connection of these three parts are well known in the art and thus not shown in detail.

[0022] The sensing stage 25 is connected at its output both to signature generator 35 and to a data multiplexer 36. Data multiplexer 36 is formed by two data pass gates 36a and 36b receiving a signature output signal TMB (and the inverted one TMBN) generated by the test mode control unit 30 so as to be alternately conductive. Data pass gate 36a is connected between the sensing stage 25 and a common output data node 37; data pass gate 36b is connected between the signature generator 35 and the common output data node 37. Common data output node 37 is connected to a buffer stage 38 in turn connected to the interface 20 to supply the input/output data I/O. The test mode control unit 30 selects one out of pass gates 36a or 36b for presenting either the sensed data outputted by the sensing stage 25 or the signature outputted by signature generator 35. The common output data node 37 which is connected to output buffers 38 and thus to the I/O pins 21e for interfacing with tester 40 can present either a signature generated by signature generator 35 or successive data sensed in sensing stage 25 of memory device 10. The sensed data can be used along with the multistrobe feature of tester 40 to perform fast speed testing. The signature can be used for testing the memory device 10 with testers that do not have the multistrobe facility.

[0023] In Figure 3, the memory device 10 is connected to a tester 40 of known type, comprising pins 41a, 41b, 41c, 41d and 41e connected to the pins 21a-21e of the memory device 10 for exchanging corresponding signals/addresses/data ALE, ADDRS, RD, CEN and I/O; a final stage control block 42 connected to the pins 41a-41e through an interface 50; a pattern generator 43; a buffer memory 44; a pattern multiplexer 45 for alternately connecting the pattern generator 43 and the buffer memory 44 to a formatter 46; and a comparator 47 having inputs connected to the final stage control block 42, to the output of the pattern multiplexer 45 and to a program memory block 48 and an output connected to an error cache memory 49.

[0024] In order to perform testing of the memory device 10 according to Figure 3, the program memory block 48 stores both the test pattern information and the

expected signature(s). Alternatively, a tester software module interacting with tester hardware may algorithmically generate the test pattern and the expected signature(s). Therefore, at the beginning, program memory block 48 sends the addresses related to the test pattern to the ADDRS pins 41b, to allow writing of the cell array 24 in a per se known manner.

[0025] Then, the tester 40 generates a random starting address, fed to the address counter 12 through the ADDRS pins 41b, 21b and latches the starting address for Burst mode reading using the ALE pins 41a, 21a. The test mode control unit 30 then replaces the external clock RD needed for synchronous reading by the internal clock CK, generating suitable values for the test mode signal TM, and controls the data multiplexer 36 to feed the buffers 38 with signature Q, instead of the read data D, generating suitable values for the signature output signal TMB. The test mode control unit 30 may also select the reading frequency, sending suitable signals to the oscillator 11.

[0026] Once the internal burst operation starts, the address counter 12 increments the addresses automatically, synchronized by the internal clock CK through burst timing control block 22 until the whole cell array 24 is scanned; then, the address counter 12 generates a last carry signal (not shown in Figure 3) sent to the test mode control unit 30, which ends testing, by switching test mode signals TM, TMN.

[0027] At each reading, the read data is supplied by the sensing stage 25 to the signature generator 35, which calculates, according to (2), the signature Q(t), formed by a 16 bit code.

[0028] At the end of reading, the end signature Q(t) is supplied through the buffers 38 and the I/O pins 21e, 41a, to the comparator 47, which also receives the expected signature from program memory block 48 and may generate a pass/fail signal P/F fed to the error cache memory 49, connected to the required tester standard output hardware (not shown) for displaying errors.

[0029] Since the successive reads are triggered internally, the multiple strobe facility provided by the tester emulates a High Speed Testing.

[0030] Figure 4 shows a more detailed scheme of the memory device 10, wherein the array 24 is divided in an even array 24a and an odd array 24b, addressed by respective even and odd decoding units 23a, 23b and read through respective even and odd sensing units 25a, 25b.

[0031] Figure 4 points out the connections between the test mode control block 30, the burst timing control block 22 and the various parts of the memory device 10, to set the required test parameters and conditions. The test mode control block 30 thus supplies a frequency control signal F_C to the oscillator 11, for setting the operating frequency thereof; the test mode signals TM, TMN to clock multiplexer 28 and burst timing control block 22 to set them in the test mode configuration; sig-

nature output signals TMB, TMBN to the data multiplexer 37 to also set them in the test mode configuration; and a signature control signal S_C (used to change the compression algorithm) to the signature generator 35. Furthermore, the test mode control block 30 receives a feedback polynomial control signal FBP_C (specifically, the present address, from which the signature control signal S_C is calculated) and a last carry signal LC (indicating that the whole matrix has been scanned) from the address counter 12. The test mode control block 30 is accessed and activated by specific commands sent to memory device 10 through ADDR5 and I/O pins 21b, 21e by tester 40, in a per se known manner, which is not shown.

[0032] As said, the burst timing control block 22 has the purpose of managing the matrix reading and generating the necessary control signals. Therefore, the burst timing control block 22, when activated by the test mode signals TM, TMN, generates increment control signals E_INC and O_INC fed to the address counter 12 for alternately incrementing the addresses of the even and odd array halves 24a, 24b; a sensing control signal E/O fed to a sensing multiplexer 57 for connecting the just read array half 24a or 24b to the signature generator 35 and to data multiplexer 37; an enable signal Enb for the data multiplexer 37; and local clock signals C_C derived from the increment control signals O_INC, E_INC for the signature generator 35. As explained with reference to Figure 3, the burst timing control block 22 is synchronized by timing clock CK', equal to internal clock CK in test mode.

[0033] The address counter 12 receives the starting address and the address latch enable signal from the ADDR5 pin 21b and the ALE pin 21a and, controlled by the increment control signals O_INC, E_INC, generates even addresses E_A or odd addresses O_A for respective even and odd decoding units 23a, 23b. The address counter 12 further generates the feedback polynomial control signal FBP_C and the last carry signal LC for the test mode control block 30.

[0034] During test mode, the test mode control block 30 receives the feedback polynomial control signal FBP_C (correlated to the present address) and generates therefrom the signature control signal S_C (thus, $S_C = f(FBP_C)$) which is thus dynamically modified during matrix reading. Since the signature is generated by modifying the feedback polynomial during linear burst, the end signature has a very high robustness against error masking.

[0035] Furthermore, in the alternative, matrix reading may be carried out twice or a number of times, and, at each scanning, the test mode control block 30 may generate different signature control signals S_C using each time a different function $f(FBP_C)$, so as to obtain different signatures, thus considerably reducing the risk of error masking. For example, S_C may be a preset bit of the present address FBP_C and, in subsequent readings, different address bits may be used.

[0036] An embodiment of the signature generator 35 using linear feedback shift registers is shown in Figure 5, which shows the implementation of an inverse filter circuit performing the function

$$f(R) = R/(1+D+D^2+D^{16})$$

or the function

$$f(R) = R/(1+D+D^2+D^{10}+D^{16})$$

wherein R is here the read data D (memory response fed by the sensing multiplexer 57) and D^i is the i-th bit of the read data D, depending upon the value of the signature control signal S_C, which may be a fixed value or a preset bit of the address of the present data D, as above explained.

[0037] Figure 5 shows in detail the structure of XOR/ADDER block 14, feedback control block 17 and master/slave unit 15. XOR/ADDER block 14 comprises an input bus 60, receiving the sixteen-bit data D (indicated as $D<15:0>$) from the sensing multiplexer 57 (Figure 4) and connected to a plurality of pass gates 61 (only one shown). The pass gates 61 (one for each bit of the read data D) receive each a respective bit and are controlled by the test mode signals TM, TMN to supply the read data to a connection bus 62 only during testing.

[0038] The connection bus 62 is connected to a first input of a plurality of EXOR gates 63.0, 63.1, ... (only two shown). Furthermore, one EXOR gate 63.0 (which receives bit $D<0>$) has a second input receiving the feedback polynomial value FBP. The other EXOR gates 63.1, ... (one for each remaining bit $D<15:1>$ of the read data D present on connection bus 62) receive, at the second input, the previous signature bits $Q<14:0>$ through a signature bus 66. Thus, the EXOR gates 63.0, 63.1, ..., receive each a respective data bit and one bit from the previous signature Q, except for the first EXOR gate 63.0 that receives FBP at the second input. The outputs of EXOR gates 63 supply a 16-bit new signature data $Din<15:0>$ to be latched which is fed to a plurality of flip/flops 64 (one shown) belonging to the master/slave unit 15. The flip/flops 64 (one for each bit of the new signature data Din) receive each a respective bit of the new signature data Din , as well as the local clock signals C_C and a reset signal R (equal for all flip/flops 64) that is used only during the start of testing for resetting the contents of the master/slave latches forming the flip/flops 64. Substantially, as shown in Figure 7, the flip/flops 64 are formed by two cascade-connected latches 80, 81 controlled by the local clock signals C_C1, C_C2, C_C2N needed for operating the latches 80, 81 in a master/slave fashion). Flip/flops 64 supply the previous signature Q stored in latch 81 to the EXOR gates 63.1, ..., and receive the new signature data Din in latch

80 in a nonoverlapping time domain synchronized with an increment clock INC fed to signature timing block 65 and given by the sum of the increment control signals E_INC and O_INC.

[0039] As shown in Figure 6, the local clock signals C_C are generated by a signature timing block 65 comprised in the burst timing control block 22 (Figure 4). Local clock signals C_C are generated from the reset signal R and the increment clock INC.

[0040] The feedback control block 17 comprises a combinatory circuit using some bits of the signature Q and the signature control signal S_C to generate the feedback polynomial value FBP. In detail, the feedback control block 17 comprises a first EXOR gate 67 having two inputs receiving two bits of the signature Q (e.g., the first and second bits Q<0>, Q<1>) and an output connected to an input of a second EXOR gate 68, a second input whereof receives a further bit of the signature Q (e.g., the last bit Q<15>). A NAND gate 69 has two inputs receiving a further bit of the signature Q (e.g., the tenth bit Q<9>) and the signature control signal S_C (as said, e.g. a preset bit of the present address), and an output connected to an inverter 70. The output of the inverter 70 is connected to an input of a third EXOR gate 71, a second input whereof is connected to the output of the second EXOR gate 68. The output of the third EXOR gate 71 thus generate the feedback polynomial value FBP.

[0041] In the example of Figure 5, the XOR/ADDER block 14 does not directly receive all the bits of the signature Q, but one less Q<15> that is instead fed indirectly from the feedback control block 17 in form of FBP. Also, the feedback control block 17 does not directly receive the read data D, differently from the general scheme of Figure 2.

[0042] In the signature generator 35, the feedback polynomial value FBP depends each time on some bits of the previous signature Q and the value of the signature control signal S_C (which also influences the function implemented by the feedback control block 17). As a consequence, the signature generator 35 acts as a filter combining each read data D supplied by input bus 60 with the previous signature Q and has an inverse filter response that changes dynamically with memory scanning. Thus, the obtained signature Q is a unique fingerprint for the pattern programmed inside the matrix 13. Furthermore, changing the signature control signal S_C in a predetermined way (so as to depend upon the present address or a combination of the addresses) reduces the chances of having two different pattern with a same signature. Moreover, matrix reading and data compression may be repeated a number of times, each time changing the signature control signal S_C so as to modify the function implemented by the signature generator 35 and to further increase the testing method robustness against error masking.

[0043] The memory device 10 may be tested in operative conditions, since the matrix 13 is read at the same

speed as during proper operation by virtue of the internal oscillator 11. Thus any criticality causing errors only at high speed may be detected. Furthermore, faults and criticalities of the memory device 10 may be detected at Wafer Sort Level testing, thus allowing device discrimination and in case rejection before packaging, eliminating useless costs. The production costs for batches are thus lower.

[0044] Finally, it is clear that numerous modifications and variations can be made to the memory and method described and illustrated herein, all of which falling within the scope of the invention, as defined in the attached claims.

[0045] In particular, the function used by the signature generator 35 may vary in subsequent matrix scanning and/or during a same matrix scanning. The variability of the functions is obtained using any parameter variable in a predefined way, e.g. depending on the matrix scan such as the address, as above described.

Claims

1. A test method for a nonvolatile memory (10), comprising the steps of:

- reading data (D) stored in memory cells (26) belonging to a memory array (24);
- generating a present signature code (Q) as a function of read data (D) and a previous signature code,

characterized by the step of receiving a value of a parameter (S_C) modifying said function and in that said step of generating a present signature code comprises generating a present signature code (Q) also as a function of said value (S_C).

2. The test method according to claim 1, characterized in that said value (S_C) is modified at each step of reading data.

3. The test method according to claim 2, characterized in that said value (S_C) is obtained from an address (A) of a memory cell (26) storing said read data.

4. The test method according to claim 3, characterized in that said value (S_C) is a bit of said address (A).

5. The test method according to claim 1, characterized in that said value (S_C) is set before beginning reading said memory cells (26) and is constant during said steps of reading and generating, and in that, at the end of said steps of reading and generating, said value is modified, the memory array (24) is read again and a different signature code (Q) is calculated as a function of the modified value.

6. The test method according to any of claims 1-5, characterized in that said function is of a polynomial type.
7. The test method according to any of claims 1-6, characterized in that said memory cells (26) of said memory array (24) are read all in linear sequence.
8. A nonvolatile memory device (10), comprising a memory array (24) including memory cells (26); means for reading (12, 23, 25) data stored in said memory cells; and a signature code generating stage (35) connected to said memory array (24) and receiving the read data (D), said signature code generating stage (35) generating a present signature code (Q) as a function of said read data and a previous signature code, characterized in that said signature code generating stage (35) has an input receiving a parameter value (S_C) and comprises variable processing elements (14, 17) controlled by said parameter value (S_C) to vary said function.
9. The device of claim 8, characterized in that said parameter value (S_C) is modified for each read data (D).
10. The device according to claim 9, characterized by address generating means (12) generating an address signal (A) for a memory cell (26) to be read and connected to said variable processing elements (14, 17) to vary said function at each data reading.
11. The device according to any of claims 8-10, characterized in that said variable processing elements (14, 17) comprise a feedback logic circuit (17) and a logic processor (14), said feedback logic circuit (17) defining a polynomial function and receiving at the input said previous signature code and said parameter value (S_C) and supplying to said logic processor (14) a feedback polynomial value (FBP).
12. The device according to claim 11, characterized in that said feedback logic circuit (17) comprises multiple input linear feedback shift registers (60-71).
13. The device according to claim 11 or 12, characterized in that said logic processor (14) comprises a plurality of EXOR gates (63.0, 63.1, ...) receiving at one input a respective bit of said read data (D), some of said EXOR gates further receiving, at a second input, selected bits of said previous signature code (Q) and at least one of said EXOR gates receiving, at a second input, said feedback polynomial value (FBP).
14. The device according to any of claims 11-13, characterized in that said signature code generating stage (35) further comprises a memory stage (15) having an input connected to the output of said logic processor (14) and an output connected to said feedback logic circuit (17) and said logic processor (14).
15. The device according to claim 14, characterized in that said memory stage (15) comprises a plurality of master/slave units (64), one for each bit of said signature code (Q).

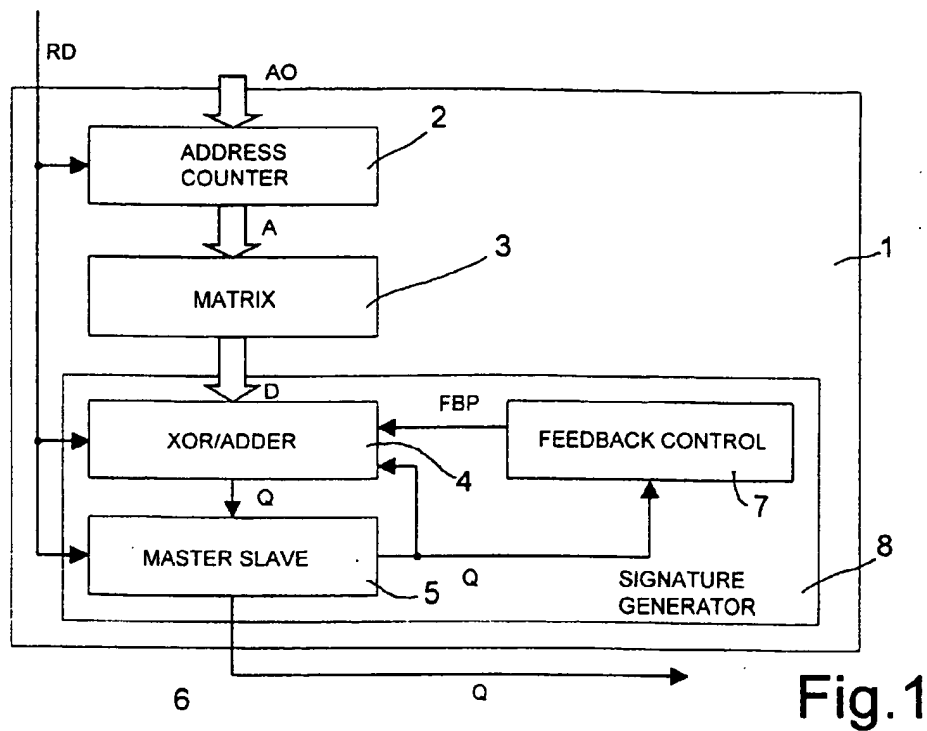


Fig.1

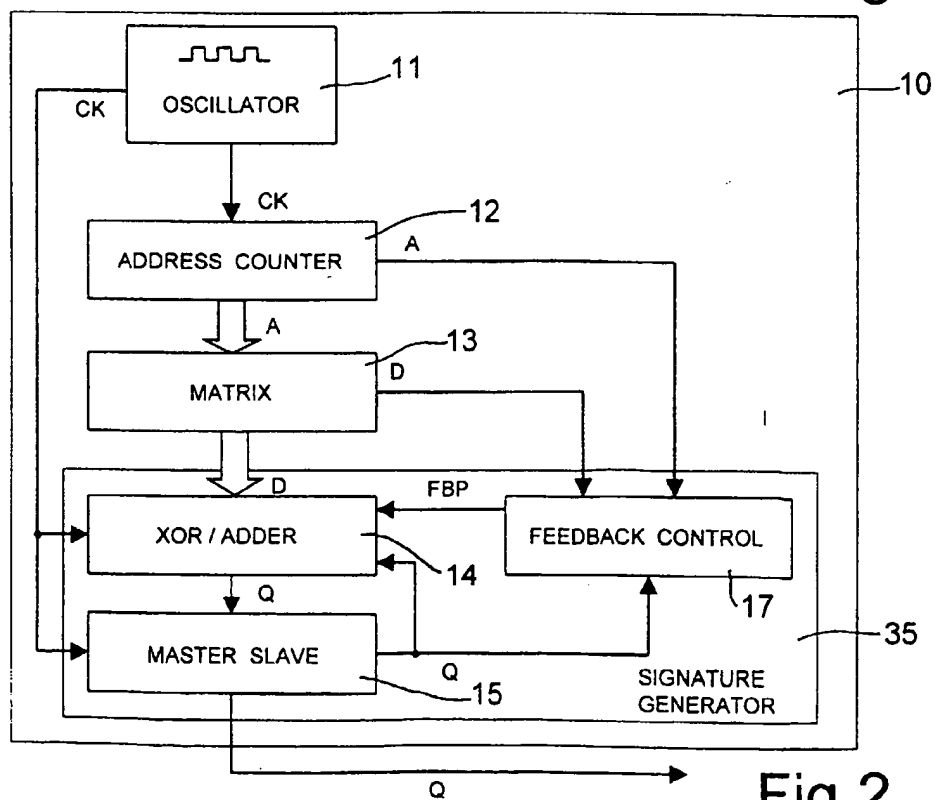


Fig.2

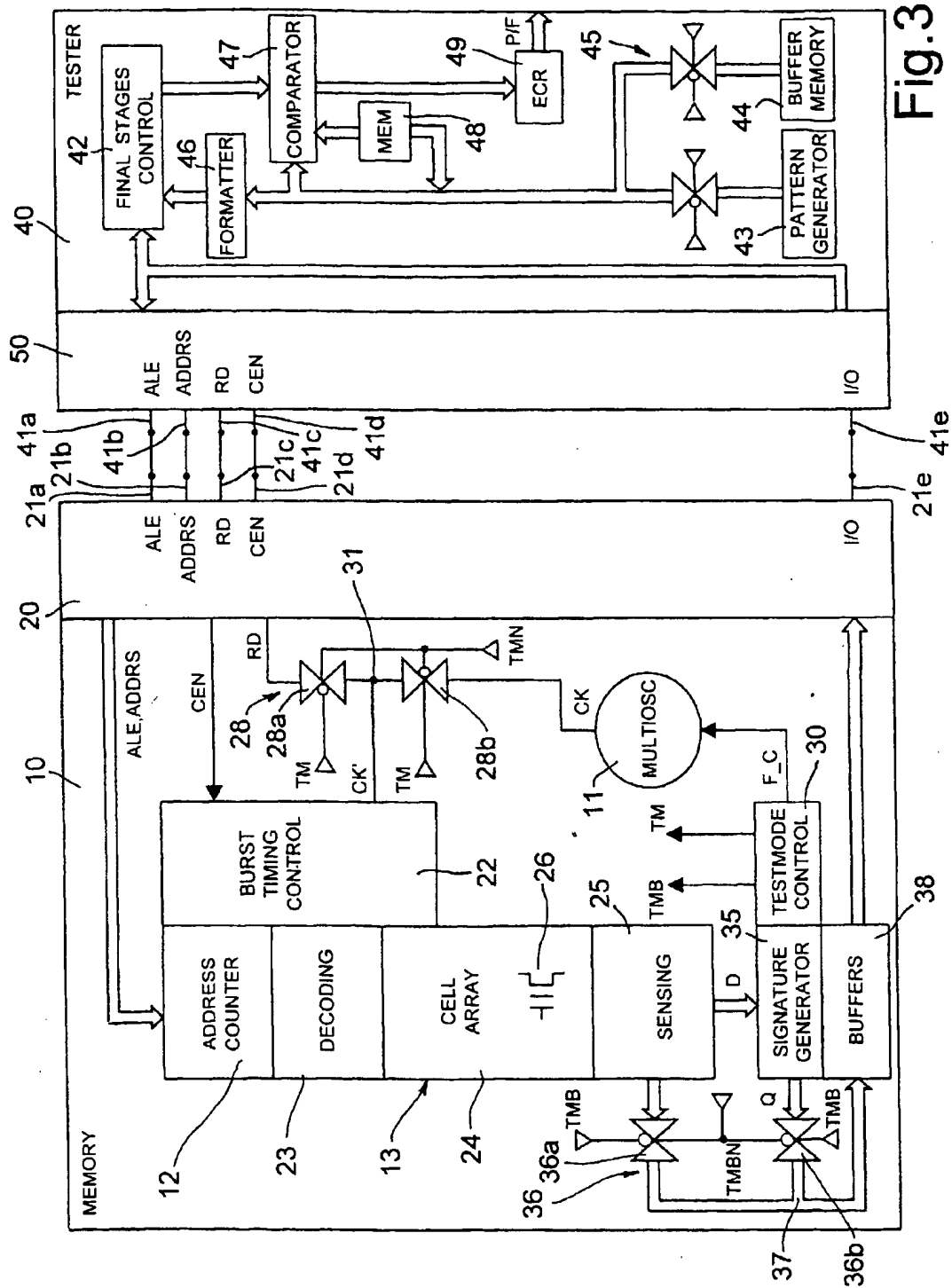


Fig.3

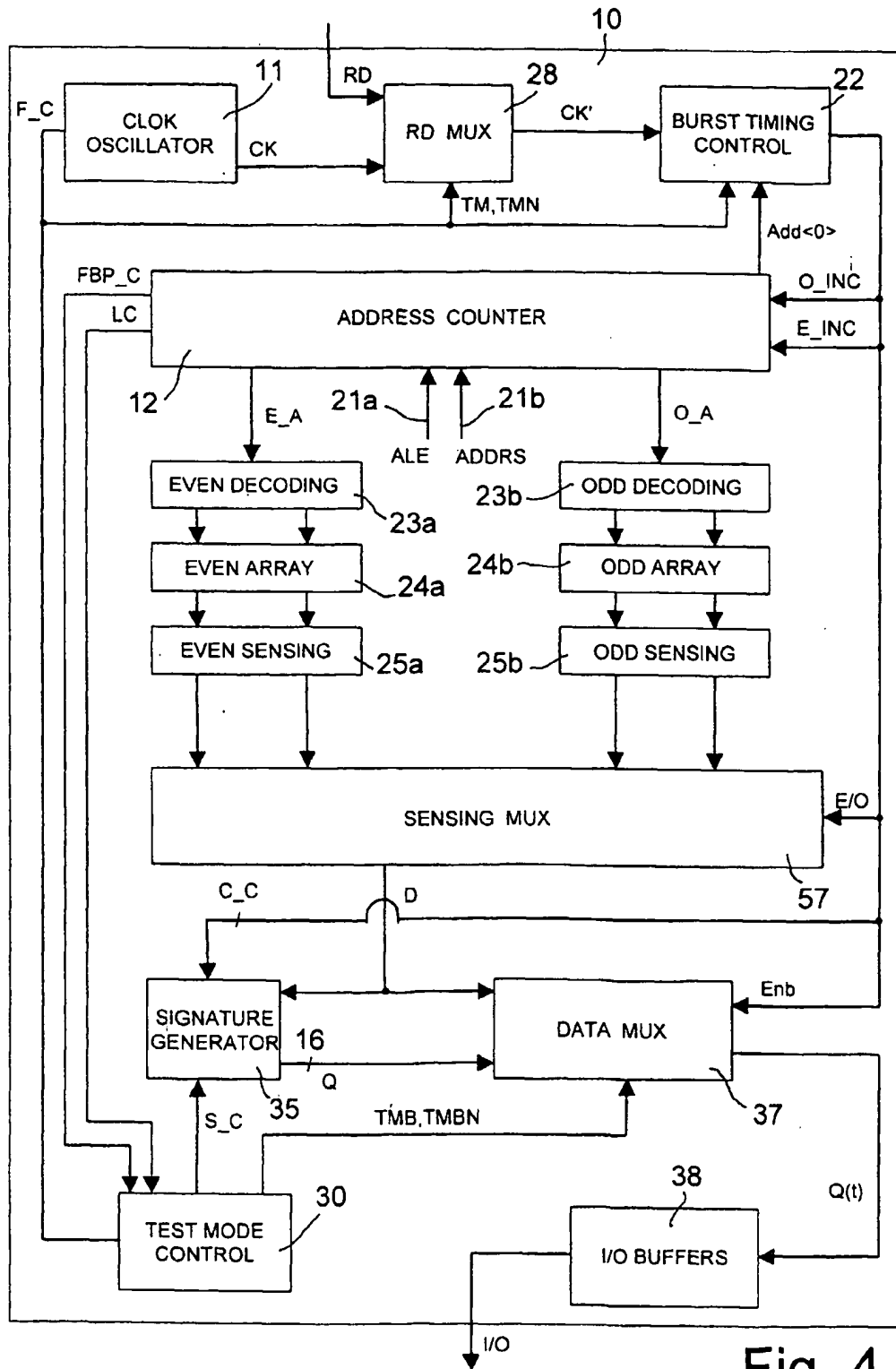
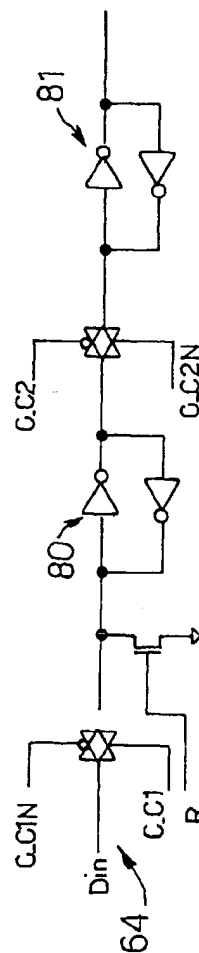
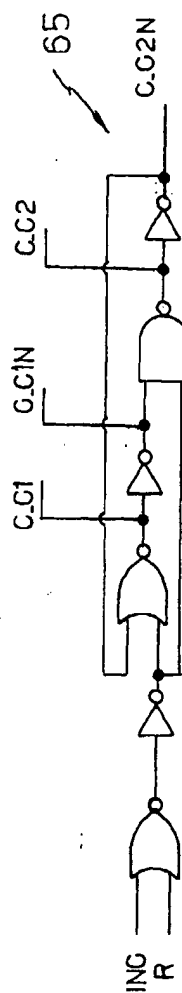
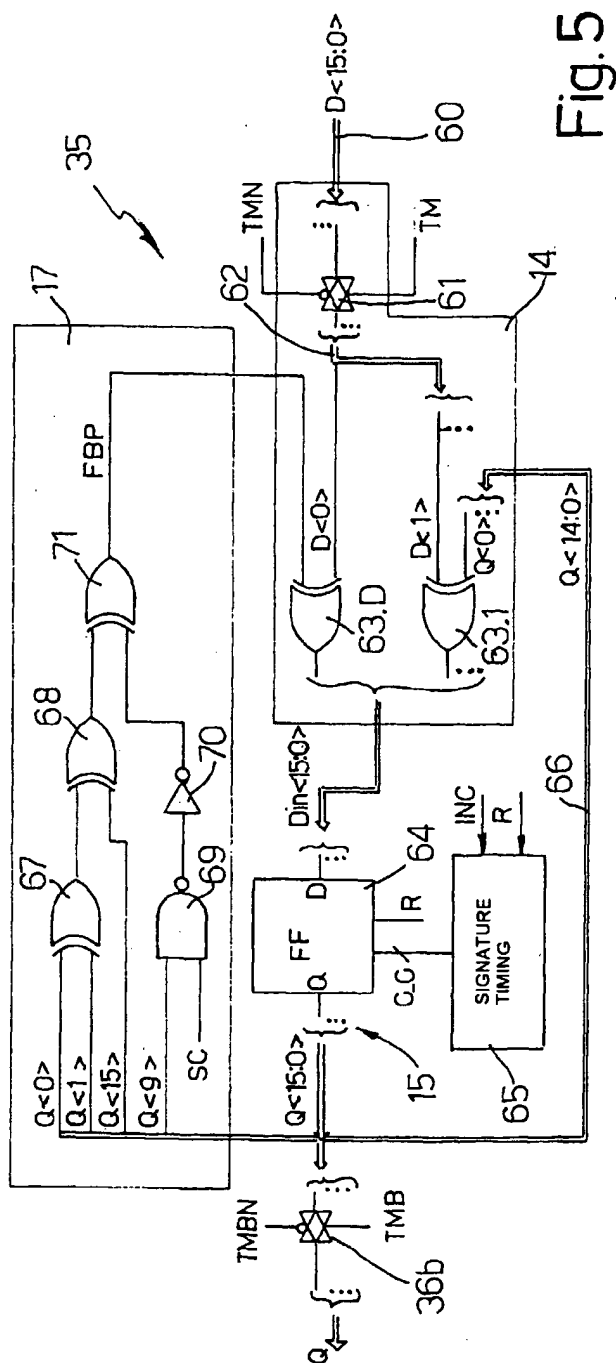


Fig. 4





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0617

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 087 (P-835), 28 February 1989 (1989-02-28) & JP 63 268199 A (NIPPON TELEGR & TELEPH CORP), 4 November 1988 (1988-11-04) * abstract; figure 4 * -----	1-15	G11C29/00
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			G11C
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 4 April 2000	Examiner Sarasua, L.
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>			

EPO FORM 1503 03/82 (P04001)

**ANNEX TO THE EUROPEAN SEARCH REPORT
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EP 99 83 0617

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
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JP 63268199 A	04-11-1988	JP 2511028 B	26-06-1996

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82